PRODUCT SPECIFICATION

MODEL: M101QC9365DA-31P

< ◇ > PRELIMINARY SPECIFICATION

< ◆ > APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED

REVISION RECORD

REV NO	REV DATE	PAGE	CONTENTS	REMARKS

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1.0 GENERAL SPECIFICATIONS

JLT101QI26228P31-28D03 is a color active matrix LCD module incorporating amorphous silicon IPS (Thin Film Transistor). It is composed of a color IPS-LCD panel, driver IC, FPC and a back light unit. The module display area contains 800*1280 pixels. This product accords with RoHS environmental criterion.

Item	Contents	Unit
Viewing direction	FULL VIEW	O' Clock
Number of Dots	800(RGB) x1280	/
Display Mode	Normally BLACK	/
Interface Type	MIPI	/
Number of color	16.7M	
LCM Luminance	240(typ)	cd/m2
Response Time (Tr+Tf)	25ms (typ)	
Contrast Ratio	250(typ)	

2.0 ELECTRICAL CHARACTERISTICS OF LCD

The following are maximum values which, if exceeded may cause fauity operation or damage to the unit.

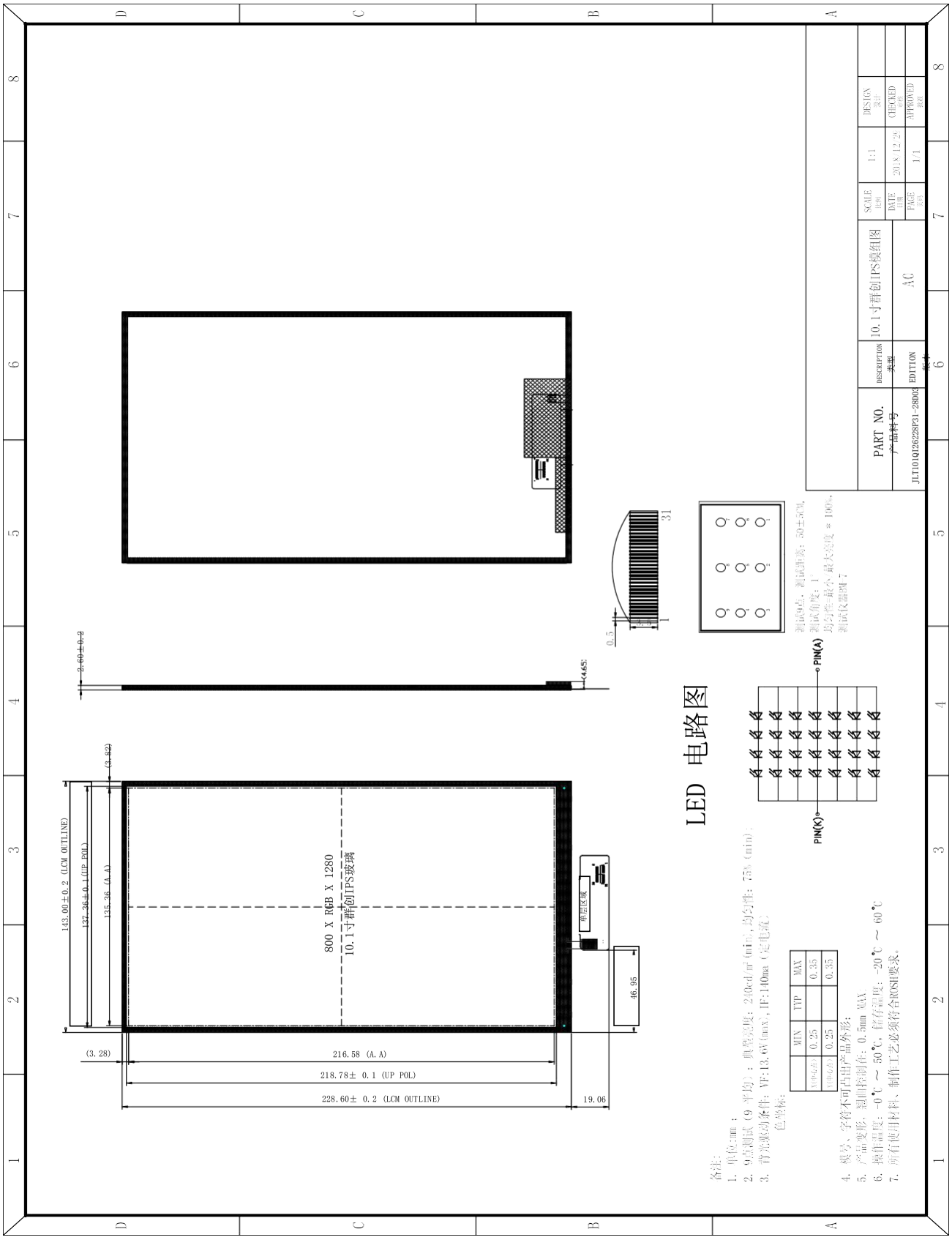
Item	Symbol	Condition	Min	TYP	Max	Unit
Digital Power Supply Voltage For LCD	**VDD**	**--**	**3.0**	**3.3**	**3.6**	**V**
Logic power Voltage	**VDDIO**	**--**	**1.7**	**1.8**	**1.9**	**V**
TFT Gate ON Voltage	**VGH**	**--**	**--**	**--**	**--**	**V**
TFT Gate OFF Voltage	**VGL**	**--**	**--**	**--**	**--**	**V**
Consumption Current Of LED	**ILED**	**VLED=12.8**	**--**	**140**	**--**	**mA**

Note: Thermal Gradient:-0.05%/℃

3.0 LED BACK LIGHT SPECIFICATION

Item	Symbol	Min	Typ	Max	Unit	Condition
Forware voltage	**Vf**	12	12.8	13.6	**V**	**If=140mA**
Forward curent	**Lf**	--	140	--	**mA**	**28-chip**
Power Consumption	**PBL**	--	**1728**	--	**mW**	**If=140mA**
Uniformity(with L/G)	**--**	75%	80%	--	--	**If=140mA**
Luminous Color	**White**					
Chip connection	28-chip 4-Serial+7-Parallel					

4.DIMENSIONAL DRAWING



5.0 INTERFACE PIN CONNECTIONS

Pin No.	Symbol	Description	Remarks
1	LED+	LED Anode	
2	LED+	LED Anode	
3	LED+	LED Anode	
4	NC	Not connection	
5	LED-	LED Cathode	
6	LED-	LED Cathode	
7	LED-	LED Cathode	
8	LED-	LED Cathode	
9	GND	Ground	
10	GND	Ground	
11	MIPI_2P	MIPI data positive signal(2P)	
12	MIPI_2N	MIPI data negative signal(2N)	
13	GND	Ground	
14	MIPI_1P	MIPI data positive signal(1P)	
15	MIPI_1N	MIPI data negative signal(1N)	
16	GND	Ground	
17	MIPI_CLKP	MIPI CLK positive signal(CLKP)	
18	MIPI_CLKN	MIPI CLK negative signal(CLKN)	
19	GND	Ground	
20	MIPI_0P	MIPI data positive signal(0P)	
21	MIPI_0N	MIPI data negative signal(0N)	
22	GND	Ground	
23	MIPI_3P	MIPI data positive signal(3P)	
24	MIPI_3N	MIPI data negative signal(3N)	
25	GND	Ground	
26	VDDIO	Logic power 1.8V	
27	RESET	Reset Pin(1.8V)	
28	GND	Ground	
29	VDDIO	Logic power 1.8V	
30	VDD	Logic power 3.3V	
31	VDD	Logic power 3.3V	

6.0 TIMING CHARACTERISTICS OF INPUT SIGNALS

6.1 Timing Characteristics

Resolution=800x1280 (T_A=25°C, IOVCC=1.8V, VCIP=VCI=VCCH=2.8V)

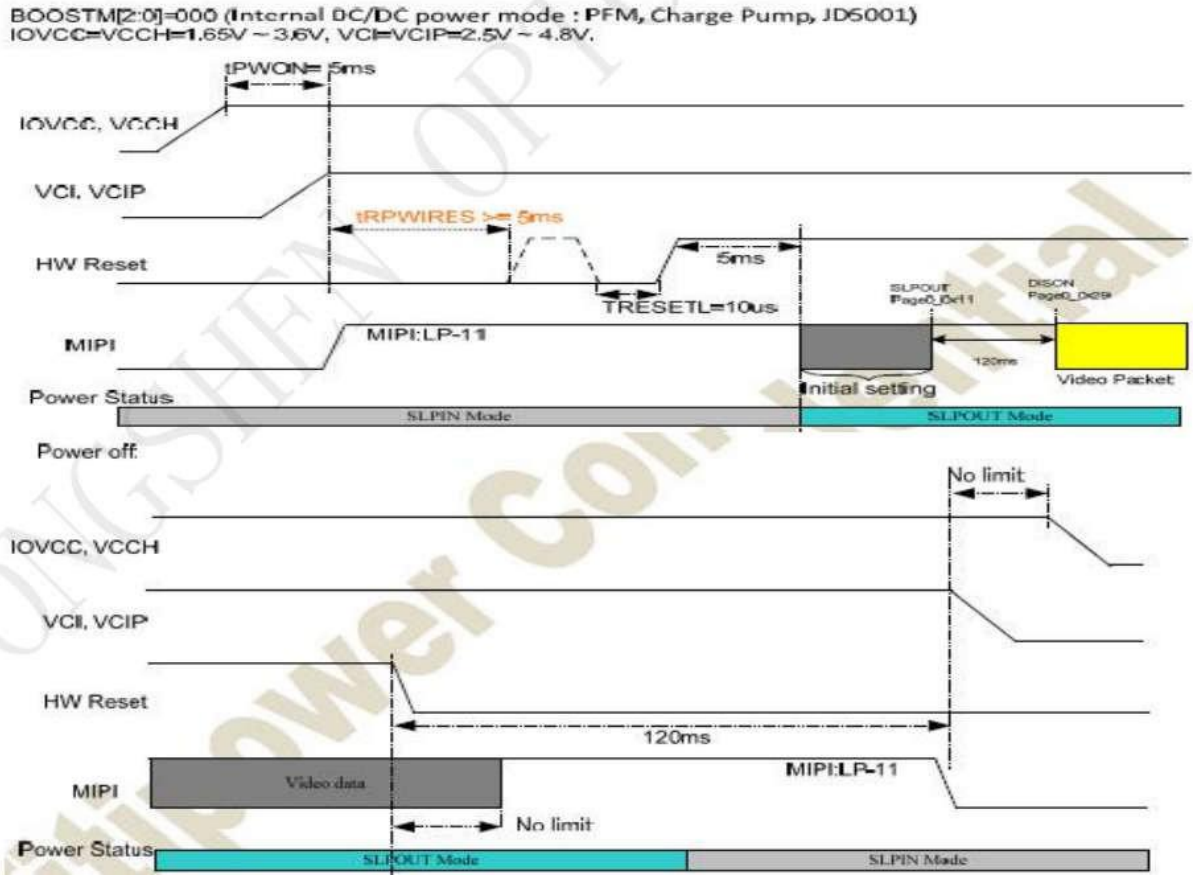
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS low pulse width	HS	-	6	18	78	DCK
Horizontal back porch	HBP	-	5	18	78	DCK
Horizontal front porch	HFP	-	5	18	78	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	16	54 (Note1)	88	DCK
Horizontal active area	HDISP	-	-	800	-	DCK
Pixel Clock	PCLK	-	63.06 (Note2)	67.33 (Note2)	81.51 (Note2)	MHz

Resolution=800x1280(T_A=25°C, IOVCC=1.8V, VCIP=2.8V, VCI=2.8V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical low pulse width	VS	-	2	4	200 Note(1)	Line
Vertical front porch	VFP	-	4	20	200	Line
Vertical back porch	VBP	-	2	10	200 Note(1)	Line
Vertical blanking period	VBK	VS+VBP+VFP	8	34	250	Line
Vertical active area	-	VDISP	-	1280	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

6.2 Power on sequence for differential power mode



```
//========== JD9365 INX T2 10.1" initial setting ==========//
Resolution:800x1280

External system porch setting:
VS=4;
VBP=8;
VFP=30;
HS=20;
HBP=20;
HFP=20;
Frame rate:60HZ

MIPI CLK:410Mbps(205MHZ);

//-----------------------Initial    Code---------------------------------- //

//Page0
SSD_Single(0xE0,0x00);

//--- PASSWORD-------//
SSD_Single(0xE1,0x93);
SSD_Single(0xE2,0x65);
SSD_Single(0xE3,0xF8);
SSD_Single(0x80,0x03);



//--- Page1-------//
SSD_Single(0xE0,0x01);

//Set VCOM
SSD_Single(0x01,0x67);

//Set Gamma Power, VGMP,VGMN,VGSP,VGSN
SSD_Single(0x17,0x00);
SSD_Single(0x18,0xBF);//4.5V, D7=4.8V
SSD_Single(0x19,0x01);//0.0V
SSD_Single(0x1A,0x00);
SSD_Single(0x1B,0xBF);
SSD_Single(0x1C,0x01);
SSD_Single(0x0C,0x74);

//Set Gate Power
SSD_Single(0x1F,0x70);      //VGH_REG=16.2V
SSD_Single(0x20,0x2D);      //VGL_REG=-12V
SSD_Single(0x21,0x2D);      //VGL_REG2=-12V
SSD_Single(0x22,0x7E);
SSD_Single(0x0C,0x74);


SSD_Single(0x35,0x28);      //SAP

SSD_Single(0x37,0x19);      //SS=1,BGR=1

//SET RGBCYC
SSD_Single(0x38,0x05);      //JDT=101 zigzag inversion
SSD_Single(0x39,0x00);
SSD_Single(0x3A,0x01);
SSD_Single(0x3C,0x7C);      //SET EQ3 for TE_H
SSD_Single(0x3D,0xFF);      //SET CHGEN_ON, modify 20140806
SSD_Single(0x3E,0xFF);      //SET CHGEN_OFF, modify 20140806
SSD_Single(0x3F,0x7F);      //SET CHGEN_OFF2, modify 20140806
```

```
//Set TCON SSD_Single(0x40,0x06);
                                    //RSO=
SSD_Single(0x41,0xA0);      //LN=640->1280 line
SSD_Single(0x43,0x1E);      //VFP=30
SSD_Single(0x44,0x0B);      //VBP=12
SSD_Single(0x45,0x28);    //HBP=40

//--- power voltage-------//
SSD_Single(0x55,0x01);
SSD_Single(0x57,0xA9);
//SSD_Single(0x58,0x0A);//////////////////////////
SSD_Single(0x59,0x0A);      //VCL = -2.5V
SSD_Single(0x5A,0x2E);      //VGH = 16.2V
SSD_Single(0x5B,0x1A);      //VGL = -12V
SSD_Single(0x5C,0x15);      //pump clk


//--- Gamma-------//
SSD_Single(0x5D,0x7F);
SSD_Single(0x5E,0x64);
SSD_Single(0x5F,0x53);
SSD_Single(0x60,0x47);
SSD_Single(0x61,0x43);
SSD_Single(0x62,0x33);
SSD_Single(0x63,0x37);
SSD_Single(0x64,0x21);
SSD_Single(0x65,0x39);
SSD_Single(0x66,0x37);
SSD_Single(0x67,0x34);
SSD_Single(0x68,0x50);
SSD_Single(0x69,0x3D);
SSD_Single(0x6A,0x44);
SSD_Single(0x6B,0x36);
SSD_Single(0x6C,0x34);
SSD_Single(0x6D,0x25);
SSD_Single(0x6E,0x15);
SSD_Single(0x6F,0x02);
SSD_Single(0x70,0x7F);
SSD_Single(0x71,0x64);
SSD_Single(0x72,0x53);
SSD_Single(0x73,0x47);
SSD_Single(0x74,0x43);
SSD_Single(0x75,0x33);
SSD_Single(0x76,0x37);
SSD_Single(0x77,0x21);
SSD_Single(0x78,0x39);
SSD_Single(0x79,0x37);
SSD_Single(0x7A,0x34);
SSD_Single(0x7B,0x50);
SSD_Single(0x7C,0x3D);
SSD_Single(0x7D,0x44);
SSD_Single(0x7E,0x36);
SSD_Single(0x7F,0x34);
SSD_Single(0x80,0x25);
SSD_Single(0x81,0x15);
SSD_Single(0x82,0x02);


//Page2, for GIP
SSD_Single(0xE0,0x02);
```

```
//GIP_L Pin mapping
SSD_Single(0x00,0x52);//RESET_EVEN
SSD_Single(0x01,0x55);//VSSG_EVEN
SSD_Single(0x02,0x55);//VSSG_EVEN
SSD_Single(0x03,0x50);//STV2_ODD
SSD_Single(0x04,0x77);//VDD2_ODD
SSD_Single(0x05,0x57);//VDD1_ODD
SSD_Single(0x06,0x55);//x
SSD_Single(0x07,0x4E);//CK11
SSD_Single(0x08,0x4C);//CK9
SSD_Single(0x09,0x5F);//x
SSD_Single(0x0A,0x4A);//CK7
SSD_Single(0x0B,0x48);//CK5
SSD_Single(0x0C,0x55);//x
SSD_Single(0x0D,0x46);//CK3
SSD_Single(0x0E,0x44);//CK1
SSD_Single(0x0F,0x40);//STV1_ODD
SSD_Single(0x10,0x55);//x
SSD_Single(0x11,0x55);//x
SSD_Single(0x12,0x55);//x
SSD_Single(0x13,0x55);//x
SSD_Single(0x14,0x55);//x
SSD_Single(0x15,0x55);//x

//GIP_R Pin mapping
SSD_Single(0x16,0x53);//RESET_EVEN
SSD_Single(0x17,0x55);//VSSG_EVEN
SSD_Single(0x18,0x55);//VSSG_EVEN
SSD_Single(0x19,0x51);//STV2_EVEN
SSD_Single(0x1A,0x77);//VDD2_EVEN
SSD_Single(0x1B,0x57);//VDD1_EVEN
SSD_Single(0x1C,0x55);//x
SSD_Single(0x1D,0x4F);//CK12
SSD_Single(0x1E,0x4D);//CK10
SSD_Single(0x1F,0x5F);//x
SSD_Single(0x20,0x4B);//CK8
SSD_Single(0x21,0x49);//CK6
SSD_Single(0x22,0x55);//x
SSD_Single(0x23,0x47);//CK4
SSD_Single(0x24,0x45);//CK2
SSD_Single(0x25,0x41);//STV1_EVEN
SSD_Single(0x26,0x55);//x
SSD_Single(0x27,0x55);//x
SSD_Single(0x28,0x55);//x
SSD_Single(0x29,0x55);//x
SSD_Single(0x2A,0x55);//x
SSD_Single(0x2B,0x55);//x

//GIP_L_GS Pin mapping
SSD_Single(0x2C,0x13);//RESET_EVEN
SSD_Single(0x2D,0x15);//VSSG_EVEN
SSD_Single(0x2E,0x15);//VSSG_EVEN
SSD_Single(0x2F,0x01);//STV2_ODD
SSD_Single(0x30,0x37);//VDD2_ODD
SSD_Single(0x31,0x17);//VDD1_ODD
SSD_Single(0x32,0x15);//x
SSD_Single(0x33,0x0D);//CK11
SSD_Single(0x34,0x0F);//CK9
SSD_Single(0x35,0x15);//x
SSD_Single(0x36,0x05);//CK7
SSD_Single(0x37,0x07);//CK5
SSD_Single(0x38,0x15);//x
SSD_Single(0x39,0x09);//CK3
SSD_Single(0x3A,0x0B);//CK1
```

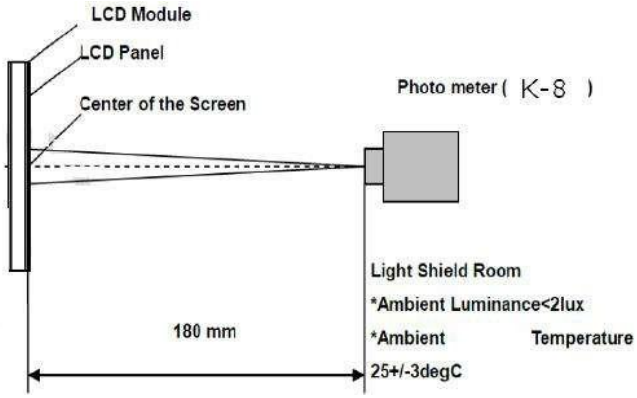
```
SSD_Single(0x3B,0x11);//STV1_ODD
SSD_Single(0x3C,0x15);//x
SSD_Single(0x3D,0x15);//x
SSD_Single(0x3E,0x15);//x
SSD_Single(0x3F,0x15);//x
SSD_Single(0x40,0x15);//x
SSD_Single(0x41,0x15);//x

//GIP_R_GS Pin mapping
SSD_Single(0x42,0x12);//RESET_EVEN
SSD_Single(0x43,0x15);//VSSG_EVEN
SSD_Single(0x44,0x15);//VSSG_EVEN
SSD_Single(0x45,0x00);//STV2_EVEN
SSD_Single(0x46,0x37);//VDD2_EVEN
SSD_Single(0x47,0x17);//VDD1_EVEN
SSD_Single(0x48,0x15);//x
SSD_Single(0x49,0x0C);//CK12
SSD_Single(0x4A,0x0E);//CK10
SSD_Single(0x4B,0x15);//x
SSD_Single(0x4C,0x04);//CK8
SSD_Single(0x4D,0x06);//CK6
SSD_Single(0x4E,0x15);//x
SSD_Single(0x4F,0x08);//CK4
SSD_Single(0x50,0x0A);//CK2
SSD_Single(0x51,0x10);//STV1_EVEN
SSD_Single(0x52,0x15);//x
SSD_Single(0x53,0x15);//x
SSD_Single(0x54,0x15);//x
SSD_Single(0x55,0x15);//x
SSD_Single(0x56,0x15);//x
SSD_Single(0x57,0x15);//x

//GIP Timing
SSD_Single(0x58,0x40);
SSD_Single(0x5B,0x10);
SSD_Single(0x5C,0x06);//STV_S0
SSD_Single(0x5D,0x40);
SSD_Single(0x5E,0x00);
SSD_Single(0x5F,0x00);
SSD_Single(0x60,0x40);//ETV_W
SSD_Single(0x61,0x03);
SSD_Single(0x62,0x04);
SSD_Single(0x63,0x6C);//CKV_ON
SSD_Single(0x64,0x6C);//CKV_OFF
SSD_Single(0x65,0x75);
SSD_Single(0x66,0x08);//ETV_S0
SSD_Single(0x67,0xB4); //ckv_num/ckv_w
SSD_Single(0x68,0x08); //CKV_S0
SSD_Single(0x69,0x6C);//CKV_ON
SSD_Single(0x6A,0x6C);//CKV_OFF
SSD_Single(0x6B,0x0C); //dummy
SSD_Single(0x6D,0x00);//GGND1
SSD_Single(0x6E,0x00);//GGND2
SSD_Single(0x6F,0x88);

SSD_Single(0x75,0xBB);//FLM_EN
SSD_Single(0x76,0x00);
SSD_Single(0x77,0x05);
SSD_Single(0x78,0x2A);//FLM_OFF
```

```
//Page4
SSD_Single(0xE0,0x04);
SSD_Single(0x09,0x11);
SSD_Single(0x0E,0x48);       //Source EQ option
SSD_Single(0x2B,0x2B);
SSD_Single(0x2D,0x03);//defult 0x01
SSD_Single(0x2E,0x44);

//Page5
SSD_Single(0xE0,0x05);
SSD_Single(0x12,0x72);//VCI GAS detect voltage

//Page0
SSD_Single(0xE0,0x00);
SSD_Single(0xE6,0x02);//WD_Timer
SSD_Single(0xE7,0x0C);//WD_Timer

//SLP OUT
SSD_Number(0x01);
SSD_CMD(0x11);         // SLPOUT
Delayms(120);


//DISP ON
SSD_Number(0x01);
SSD_CMD(0x29);         // DSPON
Delayms(5);
```

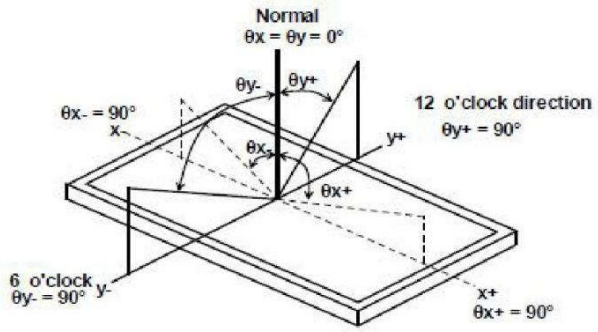
7.0 ELECTRO-OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Panel Transmittance		T	θ = ϕ 0°	4.4	4.7	--	%	
Luminance		L	θ = ϕ 0°	220	240	--	cd/m2	Note1
Luminance Uniformity		YU	9points	--	75	--	%	Note5
Contrast Ratio		CR	Point-5	--	250	--	-	Note3
Response Time		Rr+Tf	Point-5	--	25	40	ms	Note4
Viewing Angle K=Contrast Ratio>10	Horizontal	ΘL	CR＞10	--	85	--		Note2
		ΘR		--	85	--		
	Vertical	ΘU		--	85	--		
		ΘD		--	85	--	.	
Color Filter Chromaticity	Wite	X	θ = ϕ 0°	0.260	0.310	0.360		Note1
		Y		0.280	0.330	0.380		
	Red	X	θ = ϕ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	Green	X	θ = ϕ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	Blue	X	θ = ϕ 0°	TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
Color gamut (NTSC ratio					TBD		%	

Note1: Measure condition :25° c±2° c, 60±100%RH,under 10 Lux in the dark room. K-8,Viewing angle 2° .Measurement after lighting on 10 minus



Note2: Definition of Viewing Angle



Note (3) Definition Of Contrast Ratio (CR)

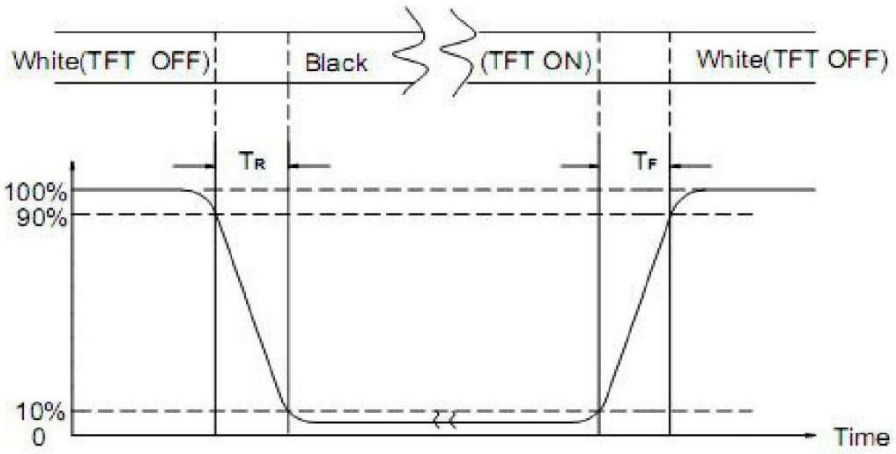
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (4) Definition Of Response Time (TR, TF)

Figure 4 Definition of Response Time



Note (5) Definition of Transmittance (Module is without signal input)

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of Back light}} \times 100\%$$

8.0 RELIABILITY
8.1 MTBF

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal. (25°C in the room without sunlight)

8.2 Tests

NO.	Test Item	Test condition	Criterion
1	High Temperature Storage	60℃±2℃ 96H Restore 2H at 25℃ Power off	
2	Low Temperature Storage	-10℃±2℃ 96H Restore 2H at 25℃ Power off	
3	High Temperature Operation	60℃±2℃ 96H Restore 2H at 25℃ Power on	
4	Low Temperature Operation	0℃±2℃ 96H Restore 2H at 25℃ Power on	
5	High Temperature & Humidity Operation	50℃±2℃ 90%RH 96H Power on	
6	Temperature Cycle	-10℃ ←25℃ 30min 5min →60℃ 30min after 10cycle, Restore 2H at 25℃ Power off	Aftertesting,cosmetic and electrical defects should not happen.
7	Vibration Test	10Hz~45Hz, 100m/s2, 120min	
8	Shock Test	Half-sinewave,300m/s2,11ms	
9	Drop Test(package state)	800mm, concrete floor,1corner, 3edges, 6 sides each time	1. After testing, cosmetic and electrical defects should not happen. 2. the product should remain at initial place 3.Product uncovered or package broken is not permitted.
10	Electro Static Discharge Test (non-operation)	150pF，330Ω，Contact:±4KV,Air: ±8KV Measure point :LCD glass and metal bezel	IEC61000-4-2：2001 GB/T17626.2-2006
		200pF，0Ω，±200V contact test Measure point :IF connector pins	

9.0 INSPECTION STANDARDS

9.1 Purpose

This incoming inspection standard shall be applied to TFT-LCD supplied by ZHONGSHEN to its customer.

9.2 Scope

This inspection standard contains Cosmetic Specifications and Electrical Specifications.

9.3 Classification of defects

9.3.1 Major defect.

The major defect is a defect that is likely to result in product failure or reduction in

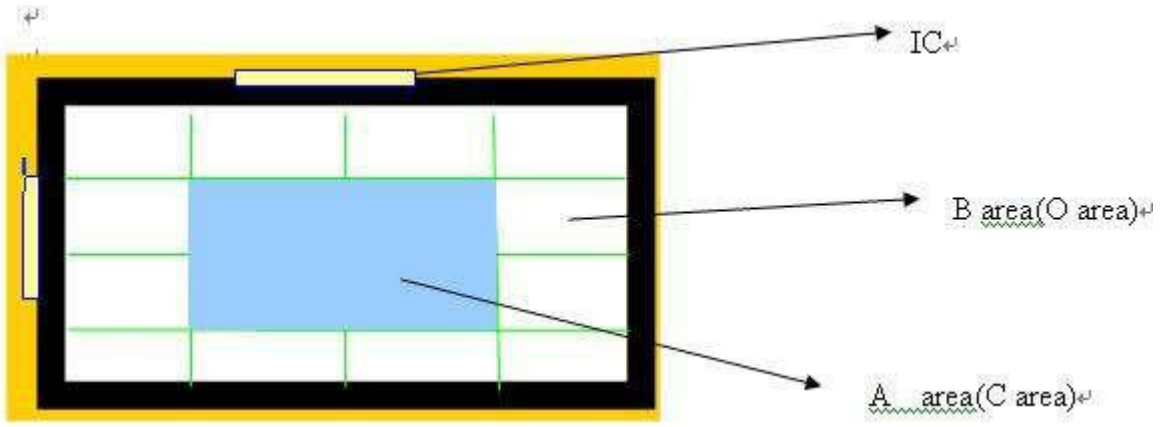
Product's intended usage.

9.3.2 Minor defect.

The minor defect is a defect that has little bearing on the effective use or Operation of the product.

9.4 Definition

9.4.1 Display area definition



9.5 Inspection conditions is as follows

9.5.1 Viewing distance is approximately 35-40 cm

9.5.2 Viewing angle is normal to the LCD panel as 45°

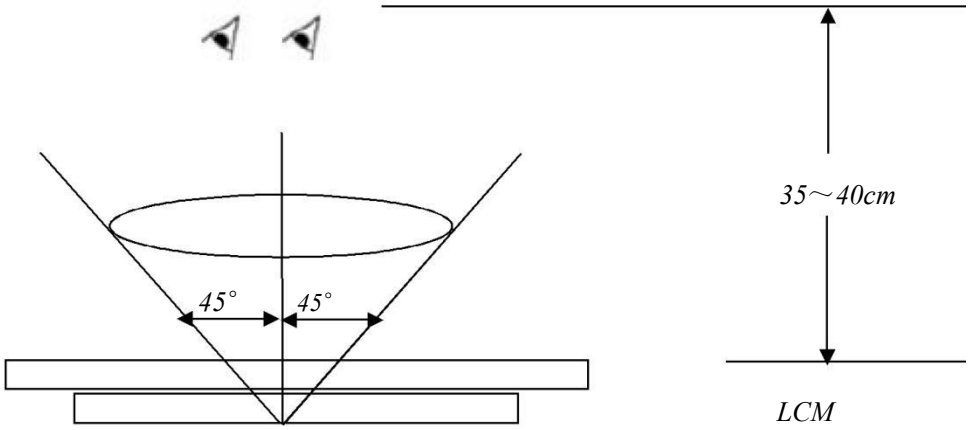
9.5.3 Ambient temperature is approximately 25±5℃

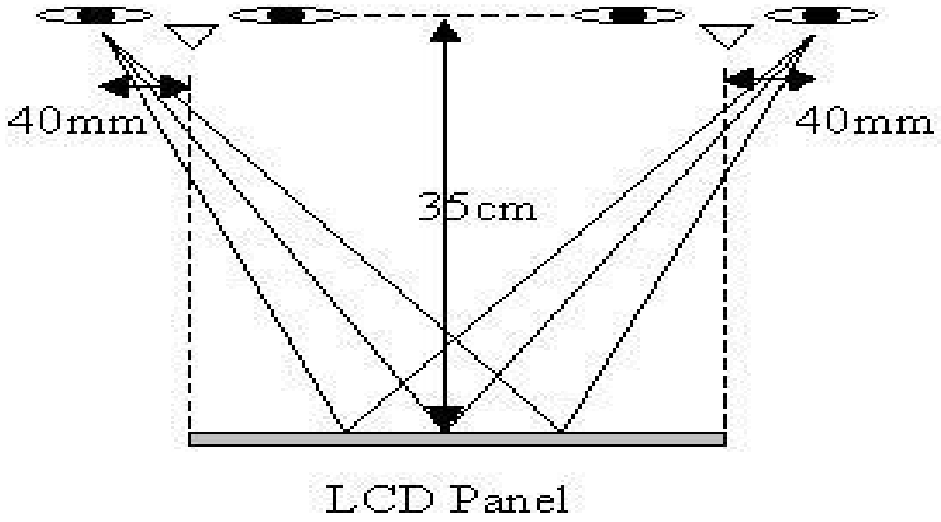
9.5.4 Ambient humidity is 60±5% RH

9.5.5 Ambient luminance is from 300-500 Lux.

9.5.6 Input signal timing should be typical value(3s-5s).

9.5.7 Mura & Light leakage inspection at ND-Filter 6%.





9.6 Sampling method

9.6.1 According to the MIL-STD-105E general inspection level , Ⅱ Sampling plan.

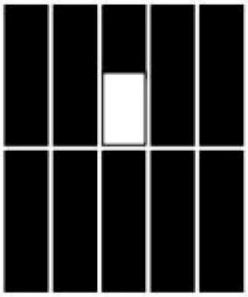
9.6.2 AQL: MA 0.65 MI 1.0

9.7 Inspection Criteria

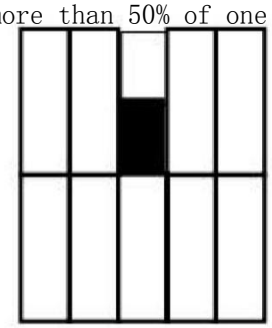
DEFECT TYPE			LIMIT			Defect	Note
VISUAL DEFECT	SCRATCH		W≤0.05mm and L≤5mm		Ignore	Maj	NOTE1
			0.05mm<W≤0.2mm L≤10mm		N≤4		
			10mm<L, 0.1mm<W		N=0		
	INTERNAL	SPOT	Φ≤0.2mm		Ignore		
			0.2mm<Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
		FIBER	0.1mm≤W≤0.2mm L≤2.5mm		N≤4		
			0.2mm<W, 2.5mm<L		N=0		
		POLARIZER BUBBLE	Φ≤0.25mm		Ignore		
			0.25mm<Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
		DENT	Φ<0.25mm		Ignore		
			0.25mm≤Φ≤0.5mm		N≤4		
			Φ>0.5mm		N=0		
ELECTRICAL DEFECT	BRIGHT DOT		C Area	O Area	Total	Maj	NOTE2 NOTE3
			N≤4（contain C area and O area）		N≤4		
	DARK DOT		N≤5（contain C area and O area）		N≤5		
	TWO ADJACENT DOT		N≤1	N≤2	N≤3		
	THREE OR MORE ADJACENT DOT		NOT ALLOWLED				
	LINE DEFECT		NOT ALLOWLED				

Note1: Minimum distance between dot defects and spot is 5mm;

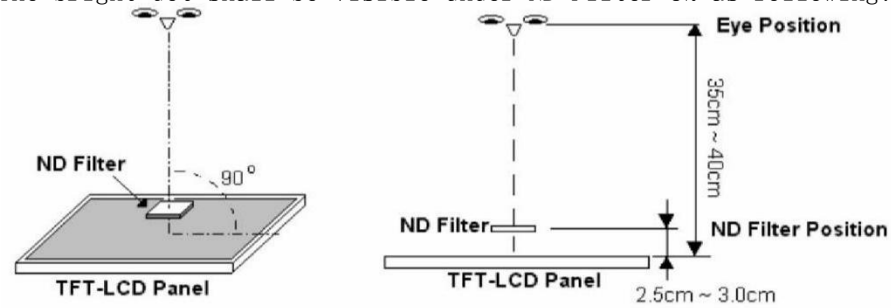
Note2: The definition of Bright dot and Dark dot -bright area is more than 50% of one dot



-dark area is more than 50% of one dot



-The bright dot shall be visible under ND-Filter 5% as following:

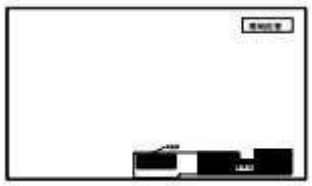


NOTE3:

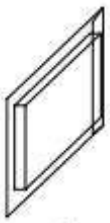
-A bit rate(bright dot model)≤10%;

-Class Chipping but not affect the function of quality OK; -Polarizing film appearance does not affect the function OK;

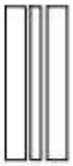
包装图:



将1PCS模组产品
装在PE袋包裹。



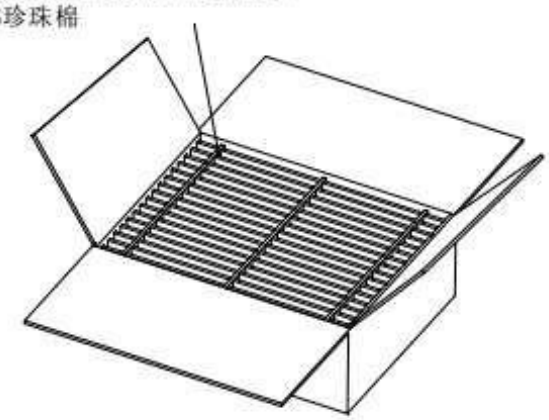
备注：2PCS产品模组的LCD
面对面，中间靠一张泡棉隔开



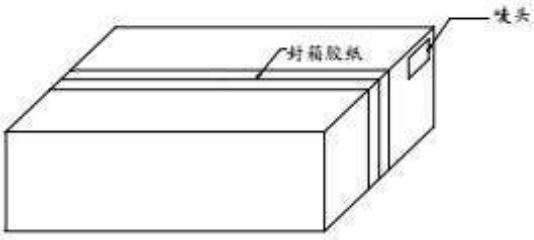
用泡棉隔开

将2PCS产品
放入纸箱里，
60pcs

在纸箱里的卡板上下两面各用
1PCS珍珠棉



使用封口胶封口
并贴附唛头



REVSION 版 本	A0	☑ 正式规格 □ 临时规格	REVISER 修订人	MODEL NO 产品料号	APPROVED BY 核 准	CHECKED BY 审 核	DRAWN BY 绘 图
DATE 日 期	2016.06.18		WG	JLT BH9050DW-30228C			
PAGE 页 码	5/6			客户:			

11.0 HANDLING PRECAUTION

(1) Don't disassemble and reassemble the module by self.
(禁止自行拆解)
(2) Acid, alkali, alcohol or touched directly by hand will damage the display.
(酸性、碱性、酒精或手的直接接触将会损伤显示面)
(3) Static electricity will damage the module. Please configure grounding device.
(静电会损伤模组，请装配接地设备)
(4)The strong vibration, shock, twist or bend will cause material damage, even module broken.
(强烈的撞击、震动、扭转或弯曲将会造成原材损伤，甚至面板破裂)
(5) It is easy to cause image sticking while displaying the same pattern for very long time.
(长期显示同一画面会造成影像残留)
(6) The response time, brightness and performance will vary from different temperature.
(响应时间、亮度与均匀性会因温度而有所改变)
(7) Starting from the date of shipment in the photoelectric products for a period of 12 months.